Department of Electronics & Telecommunications Engineering Third Year CMOS Design (BTETPE604A) Question Bank	
UNIT I	
SR.NO.	Question
1	What is threshold voltage for the MOSFET? Write its formula
2	Explain Channel Length Modulation the non-ideal effect of MOS transistor
3.	Explain how transistor work as switch?
4	Draw CMOS inverter VI characteristics & explain them
5	Draw CMOS VTC curve and explain effect of β on VTC curve
6	Explain MOSFET Level 1 and Level 2 models
7	Explain Body effect on MOSFET
8	Explain subthreshold conduction the non-ideal effect of MOS transistor
9	Explain Velocity Saturation the non-ideal effect of MOS transistor
10	Draw schematic diagram of CMOS inverter and explain its working
11	Explain how NMOS works
12	Explain how PMOS works
13	What is Noise Margin for CMOS circuits?
14	Explain various short channel effects on MOSFET
15	Derive equation for Noise Margin High and Noise margin Low
UNIT II	
1	Draw and explain NMOS fabrication
2	Draw and explain PMOS fabrication
3	Draw various steps in n-well CMOS fabrication
4	Draw various steps in p-well CMOS fabrication
5	Draw various steps in Twin-Tub CMOS fabrication
6	Write CMOS Lambda based layout design rules in detail with figures
7	Write CMOS micron-based layout design rules in detail
8	Explain various parasitic capacitors in MOSFET
9	Draw schematic of two stage CMOS inverter and explain all the parasitic capacitors and write value of load capacitor
10	Explain MOS capacitor
11	Explain MOSIS CMOS design rules
12	Explain the parasitic capacitance at layout level
13	Explain various steps involved to draw a layout
14	Draw layout for CMOS inverter
15	Draw layout for CMOS 2 input NAND gate
UNIT III	
1	What do you mean by a logical effort?
2	What is parasitic delay?
3	Explain RC delay model for CMOS inverter
4	Draw and explain linear delay model

5	Calculate logical effort required for CMOS inverter with equal rise and fall time in 65nm process
6	Calculate logical effort for two input NAND gate with equal rise and fall time.
7	Calculate logical effort for three input NOR gate with equal rise and fall time.
8	What is propagation delay?
9	Draw RC delay model for 2 input NOR gate
10	What are skewed and unskewed gates?
11	Find the logical effort required for 2 input XOR gate
12	Find the logical effort required for 2 input XNOR gate
13	What are the advantages of linear delay model over RC delay model
14	If a transistor has R=10KΩ & C=0.1fF in 65nm process, compute delay in pF of inverter with fanout 4
15	How Elmore delay is calculated?
UNIT IV	
1	Explain static and dynamic power dissipation in CMOS circuits
2	What is an activity factor?
3	What is dynamic voltage scaling (DVS)?
4	Explain Gate leakage in static CMOS circuits
5	A cache in 65nm process consumes an average power of 2 W. Estimate how wide should the PMOS header switch be if delay should not increase by more than 5%
6	What are pitfalls and fallacies for power management of CMOS circuits
7	Draw the RLC interconnect model
8	What is Skin effect?
9	Determine the skin depth for a copper wire in a chip with 20 ps edge rates
10	Explain how interconnect affect delay
11	What is crosstalk in CMOS circuits
12	Explain different process variation parameters in CMOS circuits
13	Explain different design corners in CMOS circuits
14	Explain various reliability issues involved with CMOS chip
15	What is scaling? Explain how scaling has affected robustness of the circuit
UNIT V	
1	Explain Static CMOS logic family
2	Explain dynamic CMOS logic family
3	Explain dual-rail CMOS logic family
4	Implement Y=AB+CD using static CMOS logic family
5	Implement Y=AB+CD using dynamic CMOS logic family
6	Implement Y=AB+CD using dual-rail CMOS logic family
7	Implement binary to Gray code converter using static CMOS logic
8	Implement half adder using static CMOS logic
9	Draw the layout of half adder circuit
10	Implement 4:1 multiplexer using static CMOS logic? How many transistors are required?
11	Implement 2:4-line decoder using dynamic logic
12	Draw the layout of 2-to-4-line decoder using Lambda based design rules

13	What are the advantages of dual rail logic over static CMOS logic
14	Implement Full adder circuit
15	Draw layout of Full adder circuit
UNIT VI	
1	How sequential circuit design is different from combinational circuit design
2	What are static circuits?
3	What are the delay constraints on sequencing the CMOS circuits
4	Draw SR CMOS latch. how many transistors are required?
5	Draw SR CMOS F/F. how many transistors are required?
6	Draw JK CMOS latch how many transistors are required?
7	Draw JK CMOS F/F. how many transistors are required?
8	Draw D CMOS latch. how many transistors are required?
9	Draw D CMOS F/F. how many transistors are required?
10	Draw layout of SR F/F using CMOS Lambda based design rules
11	Draw layout of JK F/F using CMOS Lambda based design rules
12	Draw layout of D F/F using CMOS Lambda based design rules
13	Draw the enabled clocked D F/F using Dynamic CMOS logic
14	Draw the layout of Q13
15	Write your observations on the case study of Pentium 4 and Itanium 2 sequencing methodologies